Results **1** - **10** of about **86,700**. (**0.21** sec)

Data appraisal, evaluation and display for synchrotron radiation experiments: hardware and software
C Boulin, R Kempf, MHJ Koch, SM ... - Nuclear Instruments and ..., 1986 - Elsevier
... The latter cycles through **16** addresses which are sent to a PROM con- taining the programming ... The **card** also carries a 30 MHz quartz oscillator from which the dot and character ... The character clock triggers the **memory** read accesses for the screen refresh and the **memory** ...
Cited by 216 - Related articles - All 2 versions

Comparing elliptic curve cryptography and RSA on 8-**bit** CPUs psu.edu [PDF]
N Gura, A Patel, A Wander, H Eberle, SC ... - ... Hardware and Embedded ..., 2004 - Springer
... Pietiläinen evaluated the relative performance of RSA and ECC on smart **cards** [**16**]. ... Unlike the CC1010, the ATmega128 implements a homogeneous data **memory** that can be addressed by three **16**-**bit** pointer registers with pre-decrement and post-increment functionality. ...
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The MIPS R10000 superscalar microprocessor toronto.edu [PDF]
KC Yeager - IEEE micro, 1996 - ieeexplore.ieee.org
... mines **memory address** dependencies in the **address** queue. ... for the Hi and Lo registers, the implic- it destinations of integer multiply and divide instructions.) These map tables have **16** read ports ... Each instruction is identified by 5-**bit** tag, which equals an **address** in the active list. ...
Cited by 751 - Related articles - BL Direct - All 37 versions

Pilchard—A reconfigurable computing platform with **memory** slot interface psu.edu [PDF]
PHW Leong, MP Leong, OYH Cheung, T Tung, CM ... - 2001 - computer.org
... The write benchmark was conducted by performing 220 = 1048576 **32**-**bit** writes to blocks of consecu- tive **memory** locations on the respective **cards**. ... In this particular example, it can be seen that **16** 64-**bit** writes are performed in approxi- mately 300 ns which equates to 426 ...
Cited by 72 - Related articles - All 13 versions

Electronic camera with **memory card** interface to a computer
K Parulski, RJ Bouvy, TJ Tredwell, DA Smith - US Patent 5,475,441, 1995 - Google Patents
... 62 SPKR o Audio Digital Waveform 63 STSCHG 0 **Card** Statuses Changed 64 D8 I/O Data **bit** 8 65 D9 I/O Data **bit** 9 66 D10 I/O Data **bit** 10 67 CD2 o **Card** detect 68 GND Ground The camera 20 is thus connected into the 68 pin PCMCIA **memory card** slot **16** of the ...
Cited by 40 - Related articles - All 3 versions

[PDF] AMBA: enabling reusable on-chip designs nthu.edu.tw [PDF]
D Flynn - IEEE Micro, 1997 - larc.ee.nthu.edu.tw
... The bank is 512 Kbytes, user-programmable, and split into two banks of emulated SRAM or ROM, each with DIP switch configuration of **32**-, **16**-, and 8-**bit**-wide **memory** with one to ... These support **16** or **32** Mbytes of bulk DRAM for large program development ... CPU daughter **card**. ...
Cited by 126 - Related articles - BL Direct - All 6 versions

The Quadrics network: High-performance clustering technology psu.edu [PDF]
F Petrini, W Feng, A Hoisie, S Coll, E ... - IEEE Micro, 2002 - ieeexplore.ieee.org
... and performance by adding communication processors on the network interface **cards** and implementing ... The **memory** management unit (MMU) translates **32**-**bit** virtual addresses into either 28-**bit** ... To translate these **address**- es, the MMU contains a **16**-entry, fully asso- ciative ...
Cited by 374 - Related articles - BL Direct - All 78 versions

Bus-to-bus bridge for a multiple bus information handling system that optimizes data transfers between a system bus and a peripheral bus
N Amini, PM Bland, BF Boury, RT Jackson - US Patent 5,499,346, 1996 - Google Patents
... CONTROLLER **CARD** SLOTS PARALLEL TIME-OF DAY CLOCK KEYBOARD PORT PERIPHERAL I/O ... 12, 1996 Sheet 4 of 7 5,499,346 31 **16** 15 AOOFt > REGISTER VRITE ... No. 08/068,477 Filed May 28, 1993 Entitled "SYSTEM DIRECT **MEMORY** ACCESS (DMA) SUPPORT ...
Cited by 72 - Related articles - All 2 versions

Eight **bit** standard connector bus for sixteen **bit** microcomputer using mirrored **memory** boards
RW Schmidt - US Patent 4,375,665, 1983 - Google Patents
... a more practical product would have both standard and mirrored buffers on the mirrored **memory card** 13, al ... unidirectional buffers 45 transpose the output 35 to the pins going to the lines **16**, and eight ... from the pins connected to the bus 15 to the input 31 to the **memory** array **32**. ...
Cited by 30 - Related articles - All 2 versions

Trends in embedded-microprocessor design psu.edu [PDF]
M Schlett - Computer, 1998 - ieeexplore.ieee.org
... 4 Another example is the MIPS **16** approach. A different approach is to use a variable instruc- tion length of, say, **16**, **32**, and 48 bits. ... RAM ROM Display/ touchscreen (various sizes supported) PC **card** slots (for example, ATA flash **memory cards**) Page 5. 48 Computer ...
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